UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,391	04/19/2004	Hideki Takahashi	252069US2	9709

22850 7590 08/02/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,391	TAKAHASHI ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *7-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/04,7/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I (claims 1-6 and 11) and species I, in the reply filed on July 5, 2005 is acknowledged. The traversal is on the ground(s) that no serious burden exists to examine all claims. This is not found persuasive because examining claims drawn to more than one patentably distinct invention and multiple patentably distinct species does impart a serious burden on the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Although Applicant did not indicate which claims read on the elected species, a quick review of the drawings indicates that claims 1-6 read on the elected species. Therefore, claims 7-11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention and/or species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 7/5/2005.

Claim Objections

Claims 2 and 3 objected to because of the following informalities:

Regarding claim 2, the limitation "said interface" is objected to. It is clear from the specification and drawings that "said interface" refers to the interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer (as defined by claim 1). However, in the context of claim 2, it appears that "said interface" could also refer to "a first interface". It is suggested the limitation "said interface" be changed to "said

interface between said second main electrode and each of said first semiconductor layer and said second semiconductor layer". Claim 3 has a similar problem.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama et al. ("Effects of Shorted...", hereinafter Akiyama) in view of Tanaka (US PGPub 2001/0040255, hereinafter Tanaka).

Regarding claim 1, Figure 1a of Akiyama discloses an insulated gate bipolar transistor (IGBT) comprising: a semiconductor substrate of a first conductivity type (n-type) including a first main surface (top surface) and a second main surface (bottom); an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region of a second conductivity type (p-type) during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate; a first main electrode (emitter electrode) formed on said first main surface and being in contact with said base region

of said insulated gate transistor at said first main surface; a first semiconductor layer (n+ short region) of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second semiconductor layer (p+ collector region) of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; and a second main electrode (collector electrode) formed on said first semiconductor layer and said second semiconductor layer; wherein an interface between said second main electrode and each of said first and second semiconductor layers is parallel to said first main surface. The difference between Akiyama and the claimed invention is a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 microns or smaller. Figure 10 of Tanaka discloses an IGBT with first and second semiconductor regions (12 and 2B, respectively) in a second main surface of a semiconductor substrate 1, wherein the thickness of the second semiconductor region 2B is less than 1 micron (approximately 0.8 microns) (paragraph [0187]). As shown in Figure 10, region 12 is thinner than region 2B, therefore the first semiconductor region 12 is also less than 1 microns. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Akiyama by using a thickness of less than 1 micron for the first and second semiconductor regions as taught by Tanaka. The ordinary artisan would have been motivated to modify Akiyama in the manner described above for the purpose of reducing the carrier injection coefficient and increasing the turn-off speed of the device (paragraph [0190] of Tanaka). Furthermore, when the thickness of the first and second semiconductor regions as taught by Tanaka is incorporated into the device of Akiyama, the

distance between said first main surface and said interface is 200 microns or smaller (190 microns + 0.8 microns).

Regarding claim 2, Figure 1a of Akiyama discloses a first interface between said first semiconductor layer (n+ short region) and said second main electrode occupies approximately 50% of said interface.

Regarding claim 3, Figure 1a of Akiyama discloses a second interface between said second semiconductor layer (p+ collector region) and said second main electrode occupies approximately 50% of said interface.

Regarding claim 4, Figure 1a of Akiyama discloses a total width of a first width (W_n) of said first semiconductor layer (n+ short region) and a second width (W_p) of said second semiconductor layer (p+ collector region) which are parallel to said first main surface and extend along a direction in which said first semiconductor layer and said second semiconductor layer are aligned is 120 microns (see Table 1, sample A).

Regarding claim 6, Figure 1a of Akiyama discloses said IGBT functions as a switching device with a built-in freewheeling diode. Note that it is inherent that the device shown in Figure 1a of Akiyama has a freewheeling diode since it has the same structure as Figure 2 of the instant application, which is disclosed as having a built-in freewheeling diode (page 14, line 10 – page 15, line 2).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama in view of Tanaka as applied to claim 1 above, and further in view of Reznik (US Pat. 6,798,040).

Regarding claim 5, a further difference between Akiyama and the claimed invention is an additional semiconductor layer of said first conductivity type which extends from an interface between said base region and said semiconductor substrate toward said interior of said semiconductor substrate, and an impurity concentration of said additional semiconductor layer is higher than that of a portion of said semiconductor substrate which forms an interface with said additional semiconductor layer. Figure 1 of Reznik discloses an IGBT with an additional semiconductor layer (buffer layer) 6 between the semiconductor substrate 1 and the base region 4, wherein the impurity concentration of layer 6 is greater than that of the substrate 1. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Akiyama by including the additional semiconductor layer (buffer layer) of Reznik for the purpose of elevating the charge carrier density in the region, thereby reducing the switching losses (col. 3, lines 4-8).

Claims 1, 2, 3, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka.

Regarding claim 1, Figure 10 of Tanaka discloses an insulated gate bipolar transistor (IGBT) comprising: a semiconductor substrate 1 of a first conductivity type (n-type) including a first main surface (top surface) and a second main surface (bottom); an insulated gate transistor formed in a region of said semiconductor substrate on a side of said semiconductor substrate where said first main surface is included, said insulated gate transistor including a channel of said first conductivity type which is formed within a base region 7 of a second conductivity type

(p-type) during an on state of said insulated gate transistor, said base region extending from said first main surface toward an interior of said semiconductor substrate; a first main electrode 11 formed on said first main surface and being in contact with said base region of said insulated gate transistor at said first main surface; a first semiconductor layer 12 of said first conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second semiconductor layer 2B of said second conductivity type formed on said second main surface of said semiconductor substrate and facing said insulated gate transistor; a second main electrode 3 formed on said first semiconductor layer and said second semiconductor layer; wherein an interface between said second main electrode and each of said first and second semiconductor layers is parallel to said first main surface, and a thickness of each of said first semiconductor layer and said second semiconductor layer is equal to 2 microns or smaller (0.8 microns) (paragraph [0187]). Tanaka does not specifically disclose a distance between said first main surface and said interface is equal to 200 microns or smaller. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a distance between the first surface and the interface equal to or less than 200 microns, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 2, Figure 10 of Tanaka discloses a first interface between said first semiconductor layer 12 and said second main electrode 3 occupies approximately 20-70% of said interface.

Regarding claim 3, Figure 10 of Tanaka discloses a second interface between said second semiconductor layer 2B and said second main electrode 3 occupies approximately 30-80% of said interface.

Regarding claim 6, Figure 10 of Tanaka discloses said IGBT functions as a switching device with a built-in freewheeling diode. Note that it is inherent that the device shown in Figure 10 of Tanaka has a freewheeling diode since it has the same structure as Figure 2 of the instant application, which is disclosed as having a built-in freewheeling diode (page 14, line 10 – page 15, line 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau